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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,426	MIL'SHTEIN ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-7 and 91-13 are objected to because of the following informalities and/or defects:

In claim 1, the recited term of "the gate voltages" lacks a sufficient antecedent basis in the claim.

In claim 1, the term of "applied" should read as: --applied to the gates--.

Claims 1, 4, 6 and 7 each recite the term of "along a channel" or "along the channel", but a channel normally has at least two dimensions, along the channel length and width directions, respectively. These claims each fail to clarify which of the channel dimensions it refers to here.

Claim 4 recited the term of "a channel," but fails to clarify its relationship with the channel already defined in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

These claims recite the subject matters of "the gate voltages being individually applied to tailor a potential along the channel of the transistor" in combination with the subject maters that the potential is "substantially uniform", and/or that "the tailoring occurs" to "create a uniform distribution of the energy subbands", and/or that the "width" of the heterostructure barrier is substantially uniform". However, the disclosure lacks an adequate description regarding how the multi-gates are individually biased (such as the relationships between the individual gate potentials), so as to achieve the above recited potential and/or subband uniformities; and/or, on how such individually biased potential relationships can be maintained when the overall bias condition changes for the gate and/or when the drain potential changes. It is not clear what are the ranges for the gate voltages applied to the respective gates, whether these voltages are different in a linear manner or non-linear manner, and/or in which direction they increase (or decrease).

In addition, it is not clear how a potential can be kept uniform in the transistor or in the channel, as the source and drain are normally at different potentials during on-state, while the channel is located between the source and drain, which makes the potential in the channel naturally non-uniform.

Furthermore, each individual gate always generates non-uniform fringe fields at the bottom edges or corners; and it is not clear how the recited uniform distribution of

energy subbands and the uniform potential recited in claims 4 and 5 can be built with the existence of such fringe fields.

Moreover, it is not clear how an electron can be accelerated by the uniform potential as recited in claim 5, since the electric field strength would be zero in such a uniform potential.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 9, 10 and 13, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Boos (Boos et al., Reduction of Gate Current in AlSb/InAs HEMTs Using A Dual Gate Design, Electronics Letters, Vol. 32, N0. 17, August 15, 1996; of record) in view of Nakagawa (US 5,313,093) and/or Brugger (US 5,405,797).

Boos discloses a heterostructured field effect transistor (Figs. 1-3; HEMT), comprising: two gates (G1 and G2; 0.5 um apart), wherein the gate voltages are individually applied to the gates to tailor the potential and/or field in the channel of the transistor.

Although Boos does not expressly disclose that the gates can have a trapezoidal cross-section, it is art known that the gate is commonly formed in trapezoidal shape, as the patterning of the gate that allows tapering of the corresponding sidewalls of the gate substantially relaxes the process conditions for the formation of the gate, also as the reduced width at the top of the gate advantageously reduces potential shortening between the gate electrode and the nearby source/drain electrodes, as evidenced in Nakagawa (see the gate 4 in the cover page figure) and/or in Brugger (see the gates 13 and 15 in the cover page figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the transistor of Boos with the gates having a trapezoidal shape, per the teachings of Nakagawa and/or Brugger, so that a transistor with relaxed process condition and/or with improved gate isolation would be obtained.

Regarding claims 2-7, it is noted that at least some of the bias conditions for the individual gates in Boos can naturally produce a substantially improved uniformities in potential (or field), in distribution of energy subbands, in width of the heterostructure barrier, and/or in the slope of the 2D electron gas barrier, compared with the case of a single-gate configuration.

Regarding claim 13, the transconductance of the transistor of Boos can be naturally substantially linear over a range of the gate voltages, compared with the case of a single-gate configuration.

5. Claims 11 and 12, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Boos in view of Nakagawa and/or Brugger, and further in view of Jan et al. ("Jean"; FR25550889; of record).

The disclosures of Boos, Nakagawa and Brugger are discussed as applied to claims 1-7, 9, 10 and 13 above.

Although Boos, Nakagawa and Brugger do not expressly disclose that the transistor can have three or four gates, one of ordinary skilled in the art would readily recognize that more gates can be desirably formed in a field effect transistor for improving the performance of the channel, a evidenced in Jean (see the individually biased multi-gates 9 in Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the transistor collectively taught above with three or four gates being formed therein, further per the teachings of Jean, so that a transistor with improved channel performance would be obtained.

Response to Arguments

6. Applicant's arguments regarding the claim rejections under 35 U.S.C. 102 and/or 103 set forth in the previous office action have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's other arguments filed on September 12, 2205 have also been fully considered but they are not persuasive. Response to theses arguments have been fully

incorporated into the claims objections and the "112"-type claim rejections set forth above in this office action.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
November 14, 2005

SHOUXIANG HU
PRIMARY EXAMINER